Module 1
Chapter 1: BJT Biasing

A *transistor* (*Bipolar Junction Transistor-BJT*) is a sandwich of one type of semiconductor (P-type or N-type) between two layers of other type. Transistors are of two types: *p-n-p transistor* and *n-p-n transistor.* There are three distinct regions (hence, terminals) in a transistor: *Emitter*, *Base*, and *Collector.*

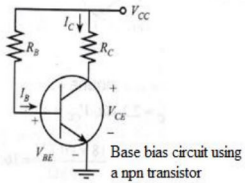
Transistor biasing is the establishment of suitable dc values such as I_C, V_{CE}, and I_B etc. by using single dc source. When BJT is properly biased, amplification of signal takes place. A transistor steady state operation depends more on its base current, collector voltage, and collector current. Therefore, if transistor is to operate as a linear amplifier, it must be properly biased to have a suitable operating point.

Establishing the correct operating point requires proper selection of bias resistor and load resistor to provide the appropriate input current and collector voltage condition. The correct biasing of transistor emitter NPN or PNP generally lies somewhere between the two extremes of operation with respect to its being either "fully-on" or "fully-off" along its load line. The central operating point is called the "**Quiescent Operating Point**" or **Q-point** for short.

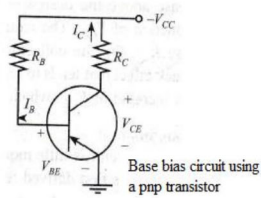
For any circuit, four-terminals would be required: two-input-terminals and two-output-terminals. Hence, for a transistor, one of the three terminals will be common to both input and output in a circuit. Thus, there are three different modes of operation for a transistor: *Common-Base Connection (CB)*, *Common Emitter Connection (CE)*, and *Common Collector Connection (CC)*. Transistor Biasing is the establishment of suitable dc-values such as IC, VCE, IB, etc., by using a dc-source. When BJT is properly biased, amplification of signal takes place. There are mainly three types of biasing a transistor: *Base bias* or *Fixed bias*, *Collector-to-Base bias*, *Voltage-divider bias*.

1.1 BASE BIAS or FIXED BIAS:

Base biasing configuration is given in the following Figure. A base resistance R_B is used between V_{CC} and base to establish the base current I_B. Since V_{CC} and R_B are fixed quantities, I_B remains fixed.



Base bias circuit using a npn transistor



Base bias circuit using a pnp transistor

Applying Kirchhoff's Voltage Law (KVL) to the base circuit:

$V_{CC} - I_B R_B - V_{BE} = 0$

Or,

$I_B = (V_{CC} - V_{BE})/R_B$ ---------- *(1)*

VBE is 0.7 V for Silicon and 0.3 V for Germanium transistor.

Applying the KVL to the collector circuit:

$V_{CC} - I_C R_C - V_{CE} = 0$

Or,

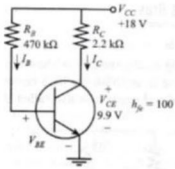
$V_{CE} = V_{CC} - I_C R_C$ ---------- *(2)*

Note that, the voltage and current polarities are reversed in base bias circuits of NPN and PNP transistors; but, the same KVL equations are applicable.

Example 1:

The base bias circuit shown in the figure, for the values indicated calculates I_B, I_C & V_{CE}

Given:



R_B=470 kΩ, R_C=2.2 kΩ, V_{CC}=18 V

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18V - 0.7V}{470\text{k}\Omega,} = \mathbf{36.8}\boldsymbol{\mu A}$$

$$I_C = h_{fe} I_B = 100 \times 36.8\mu A = \mathbf{3.68}\boldsymbol{mA}$$

$$V_{CE} = V_{CE} - I_C R_C = 18V - \left(3.68mA \times 2.2\text{k}\Omega\right) = \mathbf{9.9V}$$

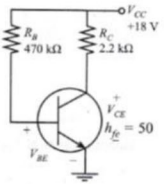
Example 2:

Calculate the mean maximum and minimum limits of IC and VCE for the base bias circuit in figure (a), when $h_{fe(min)}$=*50* and $h_{fe(max)}$=*200*.

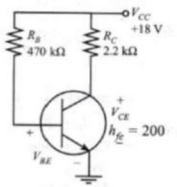
Given:

$h_{fe(min)}$=*50* and $h_{fe(max)}$=*200*.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\text{V} - 0.7\text{V}}{470\ \text{k}\Omega} = 36.8\mu\text{A}$$



(a): Conditions for $h_{fe(min)}$



(b): Conditions for $h_{fe(max)}$

Case i:

$h_{fe(max)}$=*200*

$$I_C = h_{fe} I_B = 200 \times 36.8\mu\text{A} = 7.36\text{mA}$$

$$V_{CE} = V_{CE} - I_C R_C = 18V - \left(7.36mA \times 2.2\text{k}\Omega = 1.8\text{V}\right.$$

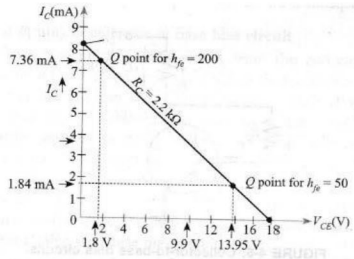
Case ii:

$h_{fe(min)}$=*50*

$$I_C = h_{fe} I_B = 50 \times 36.8\mu\text{A} = 1.84\text{mA}$$

$$V_{CE} = V_{CE} - I_C R_C = 18V - \left(1.84mA \times 2.2\text{k}\Omega = 13.95\text{V}\right.$$

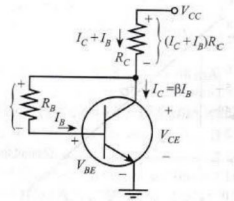
Two Q points in figure (c) for a transistor for a given type number always have a wide range of h_{fe} values (the h_{fe} spread).so $h_{fe\ (max)}$ and $h_{fe\ (min)}$ should always be used for practical analysis. This bias circuit is clearly implied because of uncertainty of the Q point. More predictable results can be obtained with other types of bias circuits.



(c): The transistor h_{fe} value has a major effect on the Q point for a base bias circuit.

1.2 COLLECTOR-TO-BASE BIAS CIRCUIT:

The collector-to-base bias circuit shown in the following Figure, has the base resistor RB connected between the transistor collector and base terminals. This circuit has significantly improved bias stability for *hfe* changes compared to base bias.



Applying KVL to the outer loop;

VCC – (IC + IB) RC – VCE = 0 Or, *VCE = VCC – (IC + IB) RC* ---------- *(3a)*

Applying KVL to the loop VCE, IBRB, and VBE;

VCE – VBE – IBRB = 0 Or, *VCE = VBE + IBRB* ---------- *(3b)*

Equating equations 3a and 3b;

VCC – (IC + IB) RC = VBE + IBRB

Or, *(IC + IB) RC + IBRB = VCC – VBE*

i.e., *IB (RC + RB) + ICRC = VCC – VBE*

Substituting $IC = \beta IB$ in above equation, we get;

IB (RC + RB) + βIBRC = VCC – VBE

Gives, *IB = (VCC – VBE)/(β+1)RC + RB* ---------- *(4)*

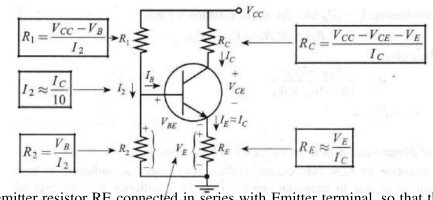
Effect of IC or β:

Any changes in VCE changes IB, the change in IB causes IC to change. If IC increases above the design level, there is an increased voltage drop across RC; resulting in reduction of VCE. The reduced VCE causes IB to be lower. If IB decreases, IC also decreases, as IC = βIB. Similarly, a reduction in IC produces an increase in VCE, which increase IB, thus tending to increase IC back to the original level. Thus an increase/ decrease in IC produces a feedback effect that tends to return IC toward its original level.

In the collector-to-base bias circuit, the feedback from the collector-to-base reduces the effect of β (due to transistor replacement). Thus collector-to-base bias has greater stability than base bias, for a given range of β values.

1.3 VOLTAGE DIVIDER BIAS CIRCUIT:

Voltage divider bias is the most stable of the three basic transistor biasing circuits. A voltage divider circuit is shown in the following figure.



There is an emitter resistor RE connected in series with Emitter terminal, so that the total dc load in series with the transistor is (RC + RE). Resistors R1 and R2 constitutes a voltage VB.

Applying KVL to the loop V_{CC}, R_1, and R_2, we get;

$V_{CC} - I_1R_1 - I_2R_2 = 0$ Or, $I_1R_1 + I_2R_2 = V_{CC}$ ---------- *(5)*

We have; $I_1 = I_2 + I_B$

Voltage divider bias circuits are normally designed to have a voltage divider current I_2 very much greater than transistor base current I_B. i.e., $I_2 >> I_B$. Hence, $I_1 \approx I_2$ ---------- *(6)*

Using 6 in 5; $I_2R_1 + I_2R_2 = V_{CC}$ *i.e.*, $I_2 (R_1 + R_2) = V_{CC}$ Or, $\boldsymbol{I_2 = (V_{CC}) / (R_1 + R_2)}$

V_B is the voltage across R_2. i.e., $V_B = I_2R_2$ Or, $\boldsymbol{V_B = (V_{CC} * R_2) / (R_1 + R_2)}$

V_E is the voltage across R_E. i.e., $\boldsymbol{V_E = I_ER_E}$

Applying KVL to the base-emitter loop; $V_B - V_{BE} - V_E = 0$ i.e., $\mathbf{V_{BE} = V_B - V_E}$

Or, $V_E = V_B - V_{BE}$ i.e., $I_ER_E = V_B - V_{BE}$ Hence, $\boldsymbol{I_E = (V_B - V_{BE}) / R_E}$

Applying KVL to the collector-emitter loop; $V_{CC} - I_CR_C - V_{CE} - I_CR_E = 0$ $[I_E \simeq I_C]$

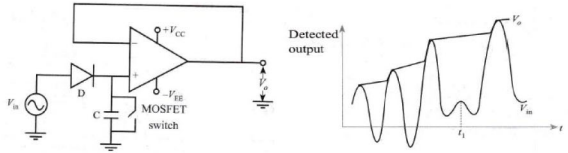
i.e., $\boldsymbol{V_{CE} = V_{CC} - I_C (R_C + R_E)}$

Module 1
Chapter 2: Operational Amplifier Application Circuit

An **Op-Amp** is a direct-coupled high gain, high bandwidth differential amplifier with very high value of input impedance and very low value of output impedance.

1.4 PEAK DETECTORS:

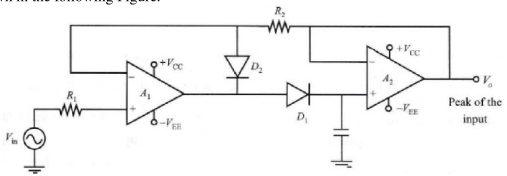
Peak detector detects holds the most positive value attained by the input signal. The following Figure shows peak detector circuit.



During positive half cycle of the input, D-conducts and capacitor charges to peak (highest) value of the input. Capacitor retains its charged value unless and until it discharges with a help of switch. The op-amp is connected as a voltage follower and its output voltage will be equal the drop across capacitor which is positive peak value of the applied voltage and will remain that for long periods until next more higher peak occurs at the input. For negative cycle of input, the diode is reverse biased and capacitor retains its value.

Modified Peak Detector:

More sophisticated peak detector that buffers the signal source from the capacitor is shown in the following Figure.



As Op-Amp (*A1*) is connected as voltage follower, the circuit presents very high impedance to the signal source. Op-Amp (*A2*) acts as a buffer between the capacitor and the load. Output (*V0*) at any given time is equal to the voltage on the capacitor which is nothing but, the peak value of the input occurred up to that time.

Whenever the input signal has higher peak than the present one, the capacitor charges up to new high input level. Whenever input level gets dropped, then capacitor retains the peak value of input, as diode *D1* gets reverse biased and diode *D2* prevents amplifier *A1* output from going into negative saturation. To hold the negative peak of the input signal, reverse the diode connections in the above figure.

Applications:

- Used for AM in communication
- Used in test and measurement instrumentation applications.

1.5 Schmitt Trigger (Regenerative Comparator)

Need for Schmitt Trigger Circuit

If the input waveform is slow or has noise on it, then there is a possibility that the output will switch back and forth several times during the switch over phase as only small levels of noise on the input will cause the output to change.

This may not be a problem in some circumstances, but if the output from the operational amplifier comparator is being fed into fast logic circuitry, then it can often give rise to problems.

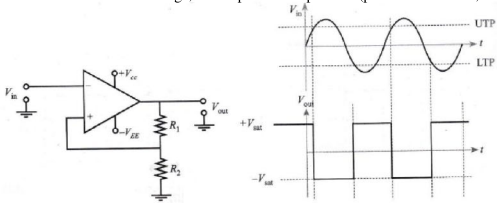
Basic Schmitt trigger circuit

A Schmitt trigger circuit is a fast-operating voltage level detector. In Schmitt trigger circit, positive feedback has an unusual effect on the circuit. It forces the reference voltage to have the same polarity as that of output voltage. The reference voltage is positive, when the output voltage is positive high ($+V_{sat}$) and negative, when the output is low ($-V_{sat}$).

Here the voltage at which the output switches from $+V_{sat}$ to $+V_{sat}$ or vice versa are called upper trigger point (UTP) and lower trigger point (LTP) and the difference between the two trigger point is called Hysteresis.

Inverting Schmitt Trigger:

The input voltage V_{in} is applied to the inverting input terminal and the feedback voltage goes to the non-inverting terminal. This means, the circuit uses positive voltage feedback (i.e., feedback voltage aids the input voltage). If the input voltage at the inverting terminal is slightly positive than feedback voltage at the non-inverting terminal, the output voltage will be negative (negative saturation, $-V_{sat}$); and if the input voltage more negative than the reference feedback voltage, the output will be positive (positive saturation, $+V_{sat}$).



Hence, the voltage at the output switches from $+Vsat$ to $-Vsat$ or vice-versa is called *Upper Trigger Point (UTP)* and *Lower Trigger Point (LTP)*. The difference between two trigger points is called *Hysteresis*. The upper and lower trigger points can be written as

$$UTP = \frac{R_2}{(R_1+R_2)} e\, V_{sat} \qquad LTP = \frac{R_2}{(R_1+R_2)} (-V_{sat})$$

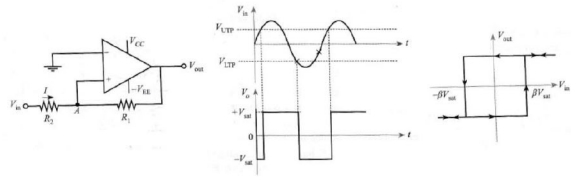
$$V_{hys} = UTP - LTP = \frac{R_2}{(R_1+R_2)} e\, V_{sat} - \frac{R_2}{(R_1+R_2)} e\, (-V_{sat}) = 2\left(\frac{R2}{R_1+R_2}\right) V_{sat} = 2\beta V_{sat}$$

$$\beta = \frac{R2}{R_1+R_2}$$

Non-Inverting Schmitt Trigger:

The input voltage *Vin* is applied to the non-inverting input terminal and the feedback voltage also goes to the non-inverting terminal. The inverting terminal is grounded.. Initially, assume that the output is in the negative saturation (*–Vsat*). Then the feedback voltage is also

negative. This feedback voltage will hold the output in negative saturation, until the input voltage becomes positive enough to make voltage positive.



Let V_A is the voltage at point *A*. Hence, $VA = IR_2$.
Since no current passes through the Op-Amp, entire current flows through R_2.

$$\text{Therefore, } I = \frac{V_0}{R_1} = \frac{+V_{sat}}{R_1}$$

When *Vin* becomes positive and its magnitude becomes greater than *(R2/R1) Vsat*, then the output switches to *+Vsat*. Therefore, the UTP at which the output switches to *+Vsat* is given by

$$UTP = \frac{R_2 V_{sat}}{R_1}$$

Similarly, when *Vin* becomes negative and its magnitude becomes greater than *(R2/R1) Vsat*, then the output switches to *–Vsat*. Therefore, the LTP at which the output switches to *–Vsat* is given by

$$UTP = -\frac{R_2 V_{sat}}{R_1}$$

$$V_{hys} = UTP - LTP = 2\left(\frac{R2}{R_1}\right)V_{sat} = 2\beta V_{sat}$$

$$\beta = \frac{R2}{R_1}$$

Applications of Schmitt Trigger:

Schmitt trigger is used in many applications, where level needs to be sensed. Hysteresis is used to reduce the multiple transitions that can occur around.

1. Digital to analog conversion.
2. Level detection.
3. Line reception.

Example 2:

Design a Schmitt trigger whose threshold voltages are ± 5 V. Draw its wave forms.

Choosing op-amp with $V_{sat} = \pm 13.5$ V with supply ± 15 V.

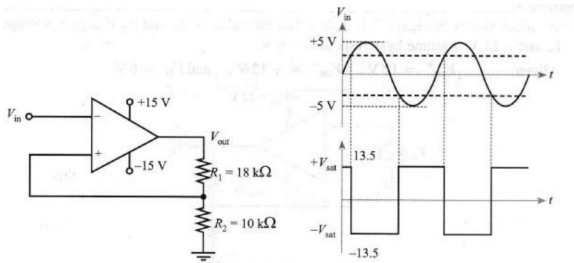
$$V_{UTP} = +5\text{ V}$$

$$\text{Now } V_{UTP} = \frac{R_2}{R_1 + R_2}.V_{sat} \quad \text{i.e., } 5 = \frac{R_2}{R_1 + R_2} \times 13.5$$

$$\therefore R_1 + R_2 = 2.7\,R_2 \quad \text{i.e. } R_1 = 1.7\,R_2$$

$$\text{Choose } R_2 = 10\,\text{k}\Omega \quad \therefore R_1 = 17\text{k}\Omega\,(\text{Use } 18\,\text{k}\Omega)$$

The designed circuit with waveform are shown below.



Example 3:

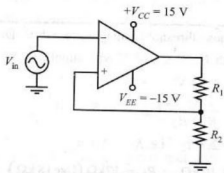
For the circuit shown, R_2 = 120 Ω and R_1 = 51 kΩ Determine the threshold voltages, if power supply applied to the op-amps are +15 V and –15 V.

Given

$$V_{sat}^{+} = +V_{CC} = +15\text{ V}.$$

$$V_{sat}^{-} = -V_{EE} = -15\text{ V}.$$

$$R_1 = 51\text{ k}\Omega, R_2 = 120\,\Omega$$



WKT

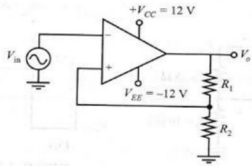
$$V_{UTP} = \frac{V_{sat}^{+} R_2}{R_1 + R_2} = \frac{15 \times 120}{51 \times 10^3 + 120} = 35.2\text{ mV}.$$

$$V_{LTP} = \frac{V_{sat}^{-} R_2}{R_1 + R_2} = \frac{-15 \times 120}{51 \times 10^3 + 120} = -35.2\text{ mV}$$

Example 4:

For the circuit shown in Figure below find the value of R_1 and R_2 if supply voltages are +12 and – 12 V. Assume hysteresis with = 6 V.

Given: $V_{sat}^{+} = 12\text{ V}$; $V_{sat}^{-} = -12\text{ V}$; and $V_H = 6\text{ V}$



Hysteresis is given by

$$V_H = \frac{R_2 V_{sat}^{+}}{R_1+R_2} - \frac{R_2 V_{sat}^{-}}{R_1+R_2} = \frac{R_2}{R_1+R_2}\left[V_{sat}^{+} - V_{sat}^{-}\right]$$

$$\therefore \frac{R_2}{R_1+R_2} = \frac{V_H}{\left[V_{sat}^{+} - V_{sat}^{-}\right]}$$

$$\therefore \frac{R_2}{R_1+R_2} = \frac{6}{12-[-12]} \qquad \therefore \frac{R_2}{R_1+R_2} = 0.25$$

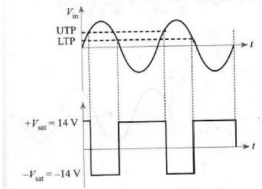
$$\therefore R_2 = 0.25R_1 + 0.25R_2 \qquad \therefore 0.75R_2 = 0.25R_1$$

$$\frac{R_2}{R_1} = \frac{0.25}{0.75} \qquad \text{Assuming } \boxed{\begin{matrix} R_2 = 10\,k\Omega \\ R_1 = 30\,k\Omega \end{matrix}}$$

Example 5:

Design Schmitt trigger circuit with UTP = 4 and LTP = 2 V [both positive] Assume V_{sat} = 14 V.

Given: V_{sat} = 14 V, UTP = 4 and LTP = 2 V.



WKT

$$V_{UTP} = \frac{R_2}{R_1+R_2}.V_{sat}$$

$$V_{LTP} = \frac{R_2}{R_1+R_2}.V_{sat}^{(-)}$$

$$V_H = V_{UTP} - V_{LTP} = 2.V_{sat}.\frac{R_2}{R_1+R_2}$$

$$= 4 - 2 = 2\times14\times\frac{R_2}{R_1+R_2}$$

$$2 = 28\frac{R_2}{R_1+R_2} \qquad 28R_2 = 2R_1+2R_2 \qquad 26R_2 = 2R_1 \qquad \text{i.e., } \boxed{R_1 = 13R_2}$$

Let $\boxed{R_2 = 10\,k\Omega}$ $\qquad R_1 = 13\times10\,k = 130\,k\Omega$

Example 6:

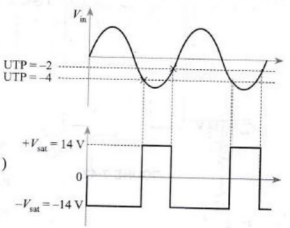
Design schmitt trigger circuit with UTP = – 2 and LTP = – 4 V. V_{sat} = 14 V.

We have, $\text{UTP} - \text{LTP} = \dfrac{2R_2}{R_1+R_2}V_{sat}$

$$-2+4 = 2 = \frac{2R_2 V_{sat}}{R_1+R_2} = \frac{2R_2}{R_1+R_2}\times 14$$

$$2 = \frac{28R_2}{R_1+R_2} \Rightarrow R_1 = 13R_2$$

Let R_2 = 10 k $\quad \therefore R_1$ = 130 kΩ (120 k std)



Also WKT

$$\text{UTP} + \text{LTP} = \frac{2R_1 V_{Ref}}{R_1+R_2}$$

$$V_{Ref} = \frac{(R_1+R_2)(\text{UTP}+\text{LTP})}{2R_1} \qquad V_{Ref} = 3.27 \text{ V}.$$

Example 7:

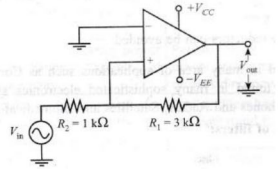
For the schmitt trigger R_1 = 3 kΩ and R_2 = 1 kΩ calculate the V_{UTP}, V_{LTP} and V_H. Assume saturation voltages as ± 12 V.

Given: $V_{sat}^+ = 12$ V; $V_{sat}^- = -12$ V; $R_1 = 2$ kΩ; $R_2 = 3$ kΩ

WKT

$$V_{UTP} = \frac{(V_{sat}^+)R_1}{R_2} = \frac{(12)\times 1\text{k}}{3\text{k}} = 4 \text{ V}$$

$$V_{LTP} = \frac{-(V_{sat}^-)R_1}{R_2} = \frac{-(12)\times 1\text{k}}{3\text{k}} = -4 \text{ V}$$



The hysteresis width is given by

$$V_H = \frac{R_1}{R_2}\left[V_{sat}^+ - V_{sat}^-\right] = \frac{1\text{k}}{3\text{k}}\left[12-(-12)\right] = \frac{24}{3} = 8 \text{ V}$$

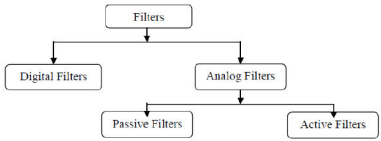
1.6 Active Filters:

INTRODUCTION:

Filter is a frequency selective circuit commonly used in signal processing that passes signal of specified range of frequencies and blocks the signals of frequencies outside the band. Active filters are attractive due to their –

- Flexibility in gain control
- Small component size
- No loading Problem
- Pass band gain
- Use of the inductors can be avoided

Filters are useful in many areas of applications, such as Communication and Signal Processing. They are found in electronic systems like Radio, Television, Telephones, Radars, satellites, and biomedical instruments.



Classification of filters

Passive filters work for high frequencies; but at audio frequencies, the inductors become problematic, as they are large, heavy, high power dissipation, and expensive.
Active filters use Op-Amp as the active element, resistors and capacitors as passive elements.

SL. No.	PASSIVE FILTERS	ACTIVE FILTERS
1	Filters with only components like resistors, capacitors, and inductors are known as passive filters.	Filters with components such as Op-Amps, transistors, and other active elements are known as active filters.
2	Passive filters do not require an external power source for operation; incapable of providing power gain.	Active filters require an external power supply for operation; capable of providing power gain.
3	Better stability and can withstand large currents.	Oscillations and noise will be generated due to feedback loops.
4	A passive filter has no frequency limitations.	Due to active elements, active filters have frequency limitations.
5	Passive filters circuits are bulky/ heavy due to the presence of inductors; they consume more power and operate with limited speed.	Active filters circuits are more compact, less heavy; and operate with high speed.
6	Difficult to fabricate in IC form and usually designed using discrete components.	Can be fabricated in IC form and usually designed using discrete components.

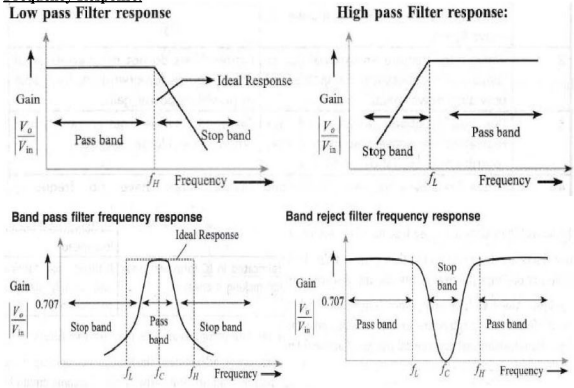
Active filters offer the following advantages over Passive filters:

- Gain and frequency adjustment flexibility
- No loading problem & No insertion loss
- Size and weight
- Cost.

Most commonly used active filters are –

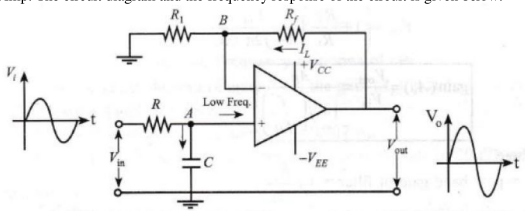
- Low-pass filter, High-pass filter, Band-pass filter, Band-stop filter (Band-reject filter), and All-pass filter.

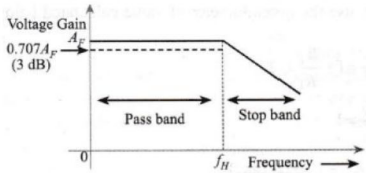
Frequency Response:



Design of Low pass filters: An active filter generally uses Op-Amp. Op-Amp has very high input impedance and low output impedance. The gain is determined by the resistive network in the feedback loop.

First Oder Active Low-Pass Filter (LPF): The first-order low-pass butter worth filter consists of a single RC filter stage, providing a low frequency path to the non-inverting input of an Op-Amp. The circuit diagram and the frequency response of the circuit is given below:





- From the graph; the gain (A_F) is almost constant for the frequency range: $0 < f < f_H$.
- At cut-off frequency, $f = f_H$, the gain is $0.707A_F$.
- After cut-off frequency f_H, the gain decreases at the rate of 20 dB/decade.
- The cut-off frequency is given by: $f_H = \frac{1}{2\pi RC}$
- Pass band gain is given by: $A_F = 1 + \frac{R_f}{R_1}$

Some applications of low-pass filters are –
- Low-pass filters are used in Audio amplifiers
- LPFs are used in equalizers or speakers to reduce the high frequency noise.

Example 1:

Design a first order low pass filter with cut-off frequency of 2.2 kHz and with pass band gain of 2.

Given: cut-off frequency $f_H = 2.2$ KHz.

Let us choose $C = 0.01$ µF.

WKT $f_H = \frac{1}{2\pi RC}$

$\Rightarrow R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi \times 2.2\times10^{3}\times0.01\times10^{-6}}$

$R = 7.233\,k\Omega$

For frequency scaling, use the potentiometer of value calculated below.

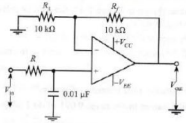
W.K.T

$A_F = 1 + \frac{R_f}{R_1} = 2$

$\frac{R_f}{R_1} = 1$

Therefore $R_f = R_1 = 10$ kΩ(Take).

The low pass filter circuit with designed values is as follows:



Example 2:

Determine the value of the resistance required for the low pass filter with cut-off frequency 30 k rad/sec and capacitor value = 0.001 µF.

Given $\omega_H = 30$k rad/sec and $C = 0.001$ µF.

WKT $\omega_H = 2\pi f_H$

and $f_H = \frac{1}{2\pi RC}$

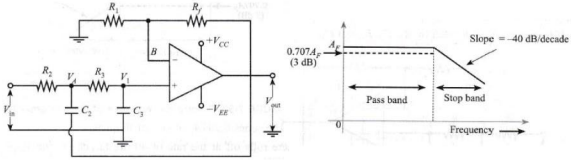
$\therefore \omega_H = 2\pi \times \frac{1}{2\pi RC} = 30\times10^{3}$

$R = \frac{1}{30\times10^{3}\times0.001\times10^{-6}}$

$= \frac{1}{30\times10^{3}\times10^{-3}\times10^{-6}} = 0.33\times10^{+5}$

$R = 33\,k\Omega$

Second Order Low-Pass Filter: First order filter can be converted to second order filter by adding an extra RC-network, as shown in the following Figure. The frequency response of second order low-pass filter is same as the first order low-pass filter except that the gain at the stop band rolls off at the rate of 40 dB/decade.



- After cut-off frequency f_H, the gain decreases at the rate of 40 dB/decade.
- The cut-off frequency is given by: $f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$
  - If $R_2 = R_3 = R$ & $C_2 = C_3 = C$; then $f_H = \frac{1}{2\pi RC}$
- Pass band gain is given by: $A_F = 1 + \frac{R_f}{R_1}$

Example 1:

Determine the values of Resistance required for second order low pass Butter worth filter having cut-off frequency as 15 k rad/sec with capacitor value as 0.01 µF.

Given: ω_H = 15 k rad/sec, C = 0.01 F.

From equation (7.38)

$$f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$$

But $R_2 = R_3 = R$ and $C_2 = C_3 = C$ and C as 0.01 µF

$$f_H = \frac{1}{2\pi\sqrt{(R)^2\times(0.01\times10^{-6})^2}} = \frac{1}{2\pi\times R\times0.01\times10^{-6}} \quad (*)$$

and $\omega_H = 2\pi f_H$ = 15 k rad/sec $= 2\pi \times f_H = 15 \times 10^3$ $f_H = \frac{15\times10^3}{2\pi}$ =2.3870 kHz

on substituting f_H in equation(*), it becomes

$$2.3870\times10^3 = \frac{1}{2\pi\times R\times0.01\times10^{-6}} \qquad R = 6.67\ \text{k}\Omega \qquad R_2 = R_3 = 6.67\ \text{k}\Omega$$

Example 2:

Design a second order low pass filter with cut-off frequency of 10 kHz and unity gain at low frequency. Also calculate the voltage transfer function magnitude at 15 kHz for the filter.

Given: Cut-off frequency $f_H = \frac{1}{2\pi RC}$

$$\therefore \quad RC = \frac{1}{2\pi f_H} = \frac{1}{2\pi\times10\times10^3} = 15.92\times10^{-6}$$

Let R = 100 kΩ, then $C = \frac{15.92\times10^{-6}}{100\times10^3}$ = 0.159 pF

Therefore C_2 = 0.159 pF and C_3 = 0.159 pF

The voltage transfer function is given by

$$\frac{V_o(s)}{V_{in}(s)} = \frac{A_F}{\sqrt{1+\left(\frac{f}{f_H}\right)^4}} = \frac{1}{\sqrt{1+\left(\frac{15\times10^3}{10\times10^3}\right)^4}} = 0.406$$

Example 3:

Design a second order low pass butter worth filter for the cut-off frequency $f_H = 200$ Hz and draw the circuit diagram.

Given : $f_H = 200$ Hz.

Choose $R_2 = R_3 = R$ and $C_2 = C_3 = C = 0.1$ μF

Now, let us find value of R

$$f_H = \frac{1}{2\pi RC}$$

$$200 = \frac{1}{2\pi \times R \times 0.1 \times 10^{-6}}$$

$$\boxed{R = 7.96\ \text{k}\Omega.}$$

For second order filter

$$R_f = 0.586R,$$

i.e $$A_F = 1 + \frac{R_f}{R_1} = 1.586.$$

choosing $R_1 = 10$ kΩ

$$1 + \frac{R_f}{R_1} = 1.586$$

$$1 + \frac{R_f}{10\ \text{k}\Omega} = 1.586$$

$$\frac{R_f}{10\ \text{k}\Omega} = 0.586$$

$$R_f = 5.86\ \text{k}\Omega$$

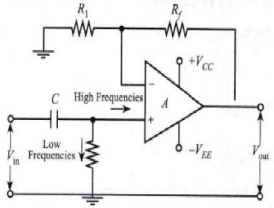
For adjustment use 10 kΩ pot.

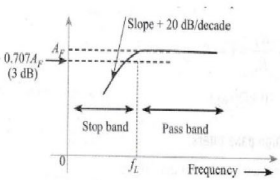
High-Pass Butter Worth Filter:

High-pass filters passes higher frequency signals, attenuating all signals below cut-off frequency, *fL*.

First Order High-Pass Butter Worth Filter:

The filter circuit consists of a passive filter followed by a non-inverting amplifier.





- At low frequency: $f < f_L$, $\frac{V_0}{V_{in}} < A_F$. A_F increases at the rate of 20 dB/decade till $f = f_L$.
- At cut-off frequency, $f = f_L$, the gain is $0.707A_F$.
- At very high frequency $f > f_L$, $\frac{V_0}{V_{in}} = A_F$ is constant.
- The cut-off frequency is given by: $f_L = \frac{1}{2\pi RC}$
- Pass band gain is given by: $A_F = 1 + \frac{R_f}{R_1}$

Example 1:

Design a first order high pass filter with a cut-off frequency of 10 kHz with pass band gain of 2.

Given: f_L = 101 kHz (given)

Choose $C < 1$ μF.

Let $C = 0.01$ μF

Calculate $R = \frac{1}{2\pi fc}$

$$R = \frac{1}{2\pi \times 10 \times 10^3 \times 0.01 \times 10^{-6}}$$

$$\boxed{R = 1.5913\ \text{k}\Omega}$$

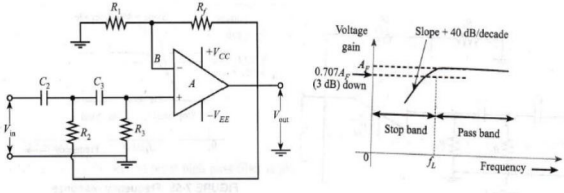
Step 4: Gain $A_F = 2 = 1 + \frac{R_f}{R_1}$

$$\therefore \quad \frac{R_f}{R_1} = 1 \Rightarrow R_f = R_1$$

Choosing R_1 = 10 kΩ(say).

Second Order High-Pass Filter:

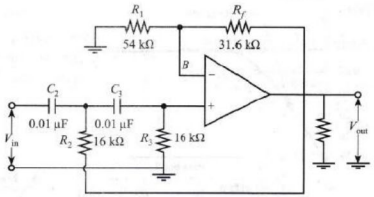
A first order high-pass filter can be converted into a second order high-pass filter by using an extra RC-network in the input side. The frequency response of second order high-pass filter is same as the first order high-pass filter except that the gain at the stop band rolls off at the rate of 40 dB/decade.



- The cut-off frequency is given by: $f_L = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$
  - If $R_2 = R_3 = R$ & $C_2 = C_3 = C$; then $f_L = \frac{1}{2\pi RC}$
- Pass band gain is given by: $A_F = 1 + \frac{R_f}{R_1}$

Example 1:

For the circuit shown in Figure find (a) lower cut-off frequency (b) pass band gain



Given: $R_2 = R_3 = 16\ \text{k}\Omega$ and $C_2 = C_3 = 0.01\ \mu\text{F}$

(a) The lower cut-off frequency for second order high pass filter is given by

$$f_L = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}} = \frac{1}{2\pi\sqrt{\left(16\times10^3\right)^2\left(0.01\times10^{-6}\right)^2}} = 1\,\text{kHz}$$

$$\boxed{f_L = 1\,\text{kHz}}$$

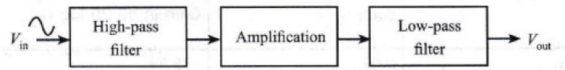
b) The pass band gain is

$$A_F = 1 + \frac{R_f}{R_1} = 1 + \frac{31.6\times10^3}{54\times10^3} = 1.586$$

$$\boxed{A_F = 1.586}$$

Active Band-Pass Filter:

Active band-pass filters provide an effective means of making a filter to pass only a given band of frequencies. An active band-pass filter can be constructed by cascading a single low-pass filter with a single high-pass filter, as shown below:

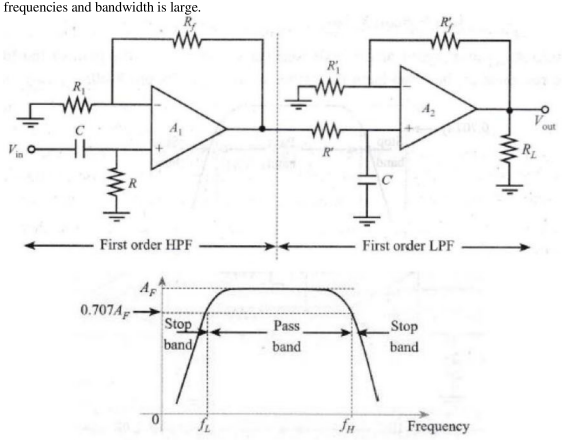


The cut-off frequency of the low-pass filter is higher than the cut-off frequency of the high-pass filter; and the difference between these frequencies at the –3dB point will give the '*bandwidth*' of the band-pass filter. A band-pass filter can be characterized by Quality factor (Q). The relation between Q, 3dB bandwidth, and the center frequency, f_C, is given by:

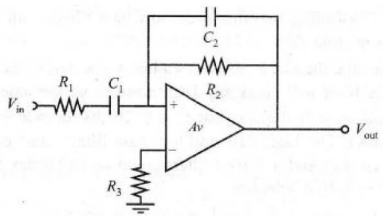
$$Q = \frac{f_c}{BW} = \frac{f_c}{f_H - f_L}$$

Wide Band-Pass Filter:

A low *Q*-filter will have a wide-pass-band; i.e., with $Q < 10$. It has wide flat response over the range of frequencies and bandwidth is large.



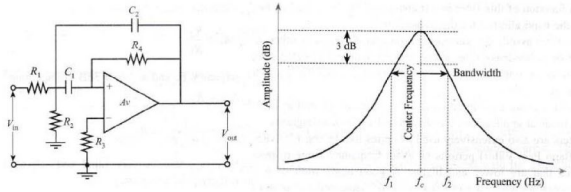
Single stage first order Band-Pass Filter:



Narrow Band-Pass Filter:

A high *Q*-filter will have a narrow-pass-band; i.e., with $Q > 10$. It has a sharp bell type response, with high gain and high selectivity.

- $fc = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$
- $Q_{BP} = \frac{f_C}{BW_{3dB}} = \frac{1}{2}\sqrt{\frac{R_1}{R_2}}$
- Maximum Gain, $A_v = -\frac{R_2}{2R_1} = -2Q^2$



Applications of Band-Pass Filters (BPF):

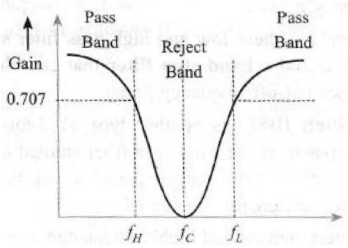
- BPFs are also used in optics like Lasers, LIDARS, etc.
- BPFs are extensively used in wireless transmitters and receivers.
- BPFs are used in electronic devices like Sonar, Seismology; and medical applications like ECG, and electrocardiograms.
- BPFs are extensively used for Audio signal processing, where a particular range of frequencies of sound is required while removing the rest.

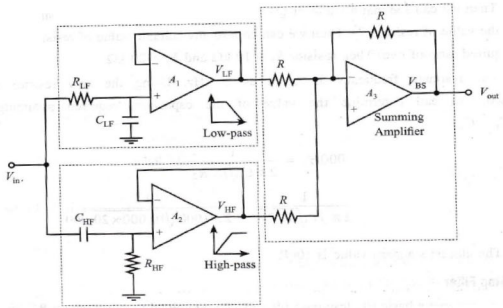
Band-Stop Filter (Band-Reject Filter):

Band-Stop Filer (BSF) is another type of frequency selective circuit that functions in exactly opposite to the band-pass filter. BSF passes all frequencies with the exception of those within a specified stop band, which are attenuated. If this stop band is very narrow and highly attenuated over a few hertz, then the band-stop filter is referred as a *notch filter*.

Wide Band-Reject Filter:

The frequency response curve and the circuit diagram of a wide band-reject filter is given below.





Example 2

Design a basic wide band, RC band stop filter with a lower cut-off frequency of 200Hz and a higher cut-off frequency of 800Hz. Find the geometric center frequency, -3dB bandwidth and Q of the circuit.

Given: $f_L = 200Hz, \quad f_H = 800Hz$

We have

$$f = \frac{1}{2\pi RC} \text{Hz}$$

The upper and lower cut-off frequency points for a band stop can be found using the same formula as that for both low and high pass filters.

Assuming a capacitor, C value for both filter sections of 0.1μF, the Values of the two frequency determining resistors, R_L and R_H are calculated as follows.

High pass filter section **Low pass filter section**

$f_L = \frac{1}{2\pi R_L C} = 200Hz \text{ and } C = 0.1\mu F$ $f_H = 2\pi \frac{1}{2\pi R_H C} = 800Hz \text{ and } C = 0.1\mu F$

$\therefore R_L = \frac{1}{2\pi \times 200 \times 0.1 \times 10^{-6}} = 7958\ \Omega \text{ or } 8K\Omega$ $\therefore R_H = \frac{1}{2\pi \times 800 \times 0.1 \times 10^{-6}} = 1990\ \Omega \text{ or } 2K\Omega$

From this we can calculate the geometric center frequency, f_C as:

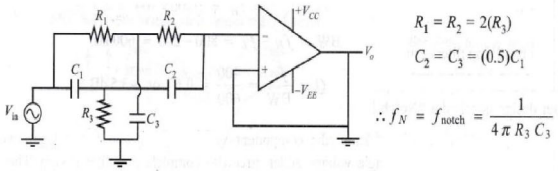
$f_c = \sqrt{f_L \times f_H} = \sqrt{200 \times 800} = 400Hz$

$BW = f_H - f_L = 800 - 200 = 600Hz$

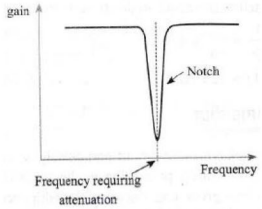
$Q = \frac{f_C}{BW} = \frac{400}{600} = 0.67 \text{ or } -3.5dB$

Narrow Band-Stop Filter (Notch Filter):

Notch filters are highly selective, high-*Q* form of band-stop filter, which can be used to reject a single or very small band of frequencies. The most common notch filter design is the twin-T notch filter network (shown below).



A twin-T network offers very high reactance at the resonance frequency and very low reactance at frequency off-resonance. In the circuit diagram, very low frequency signals find their way to the output via low-pass filter (formed by R1 – R2 – C3); and very high frequency signals find their way to the output via high-pass filter (formed by C1 – C2 – R3). Hence, in an intermediate band of frequencies, both filters pass signals to the output; due to cancellation of +ve phase shift of high-pass filter with the –ve phase shift of the low-pass filter.



Example 1:

Design a two op-amp narrow-band, RC notch filter with a center notch frequency, f_N of 1kHz and a -3dB bandwidth of 100Hz. Use 0.1μF capacitors in your design and calculate the expected notch depth in decibels.

Given: $f_N = 1000Hz, BW = 100Hz \; and \; C = 0.1\mu F.$

1. Calculate value of R for the given capacitance of 0.1μF

$$R = \frac{1}{4\pi f_n C} = \frac{1}{4\pi \times 1000 \times 0.1 \times 10^{-6}} = 795\Omega \; or \; 800\Omega$$

2. Calculate the value of Q.

$$Q = \frac{f_N}{BW} = \frac{1000}{100} = \frac{1000}{100} = 10$$

3. Calculate the value of feedback fraction k

$$K = 1 - \frac{1}{4Q} = 1 - \frac{1}{4 \times 10} = 0.975$$

4. Calculate the values of resistors R_3 and R_4

$$K = 0.975 = \frac{R_4}{R_3 + R_4}$$

Assume R_4= 10kΩ, then R_3 equals:

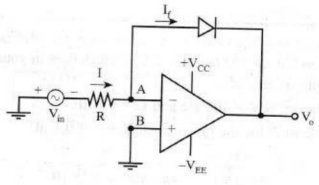
$$R_3 = R_4 - 975\ R_4 = 10000 - 0.975 \times 10000$$
$$\therefore R_3 = 250\Omega$$

5. Calculate the expected notch depth in decibels,(dB)

$$\frac{1}{Q} = \frac{1}{10} = 0.1$$
$$f_{n(dB)} = 20\log(0.1) = -20\ dB$$

1.7 NON LINEAR AMPLIFIER:

Non linearity is the behaviour of a circuit, particularly an amplifier, in which the output signal strength do not vary in direct proportion to the input signal strength. A non-linear amplifier in as circuit which gives non-linear relationship between its input and output signals. The Non-linear amplification can be achieved in a simple way by just connecting a non-linear device such as PN-junction diode in the feedback path. In the circuit shown is the following Figure, large change in input voltage causes small change in the output voltage. This circuit is a log amplifier; hence the output voltage is logarithm of the input voltage.



The above Figure shows a non-linear amplifier, where diode '*D*' is used in negative feedback path. By virtual ground concept; as node *B* is grounded, node *A* will be virtually grounded. Therefore, $V_A = 0$.

We have; $I = \frac{V_{in} - V_A}{R} = \frac{V_{in}}{R}$ since $V_A = 0$.

Let I_f be the current through the diode. The voltage across diode is *VA – V0*. Since, *VA = 0*, the voltage across diode is *–V0*.

Diode equation: $-V_0 = \eta V_T \ln\left[\frac{I_f}{I_r}\right]$

Where, *VT* – Voltage equivalent of Temperature
If – Diode forward current
Ir – Diode reverse saturation current.
Since, current through the Op-Amp is negligible; $I = I_f$
Therefore, $I_f = I = \frac{V_{in}}{R}$

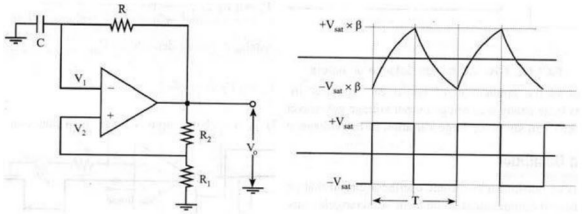
Gives, $V_0 = \eta V_T \ln\left[\frac{V_{in}}{I_r R}\right] = \eta V_T \ln\left[\frac{V_{in}}{V_{ref}}\right]$ $I_r, R = V_{ref}$ is a constant.

The above equation shows that, the output voltage is a logarithmic function of input voltage.

Applications:
Non-linear Amplifiers are used in AC bridge balance detectors.

1.8 RELAXATION OSCILLATOR:

Relaxation oscillator is a non-linear electronic oscillator circuit that generates a continuous non-sinusoidal output signal in the form of rectangular wave, triangular wave or a saw-tooth wave. The time period of non-sinusoidal output depends on the charging time of the capacitor connected in the oscillator circuit. The relaxation oscillator basically contains a feedback loop that has a switching device in the form of transistor, relays, operational amplifiers, comparators, or a tunnel diode that charges a capacitor through a resistance till it reaches a threshold level then discharges it again. The following Figure shows the basic circuit of an Op-Amp based relaxation oscillator.



Assume that, the output is initially in positive saturation. As a result, voltage at non-inverting input of Op-Amp is $+V_{SAT} * R_1 / (R_1 + R_2)$. This force the output to stay in positive saturation as the capacitor C is initially in fully discharged state. Capacitor C starts charging towards $+V_{SAT}$ through R. The moment the capacitor voltage exceeds the voltage appearing at the non-inverting input, the output switches to $-V_{SAT}$.

Now, the voltage appearing at the non-inverting input changes to $-V_{SAT} * R_1 / (R_1 + R_2)$. The capacitor starts discharging and after reaching zero, it begins to discharge towards $-VSAT$. Again, as soon as it becomes more negative than the voltage appearing at the non-inverting input of the Op-Amp, the output switches back to $+V_{SAT}$.

The expression for the time period of the output rectangular waveform is given by;

$$T = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

In the above equation, the natural logarithm is used, which is logarithm to base e. By varying the value of resistorR, the time period of the output waveform can be varied.

β is the feedback fraction/ factor and is given by $\beta = R_1 / \left(R_1 + R_2\right)$

When the output voltage V_0 is at at $+V_{SAT}$ the feedback voltage is known as upper threshold voltage V_{UTP} and is given by $+V_{SAT} \times R1\left(R1 + R2\right)$

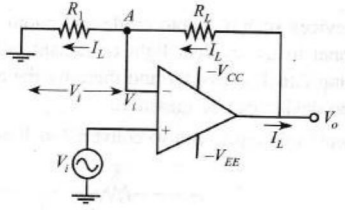
When the output voltage V_0 is at at -VSAT the feedback voltage is known as lower threshold voltage V_{LTP} and is given by $-V_{SAT} \times R1\left(R1 + R2\right)$

1.9 VOLTAGE TO CURRENT (V TO I) CONVERTER:

In many applications, we have to convert a voltage to a proportionate current. These voltage-to-current converter circuits can be of *two types*:

a) **Voltage to Current Converter with Floating Load:**

The circuit is shown in the following Figure, where *RL* is the floating load.

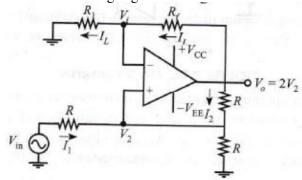


Since, voltage at node A is V_i; $V_i = I_L R_1$ Or, $I_L = \frac{V_i}{R_1}$

i.e., input voltage V_i is converted into and output current.

b) **Voltage to Current Converter with Grounded Load:**

The circuit is shown in the following Figure.



$I_1 = \frac{V_{in} - V_2}{R}$, $I_2 = \frac{V_0 - V_2}{R}$

The load current is given by; $I_L = I_1 + I_2$

Therefore, $I_L = \frac{V_{in} - V_2}{R} + \frac{V_0 - V_2}{R} = \frac{V_{in} + V_0 - 2V_2}{R}$

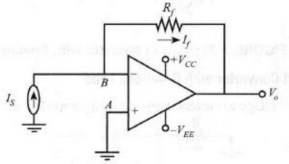
For a non-inverting amplifier, we know that; $A_v = 1 + \frac{R}{R} = 2$ $so, V_0 = 2V_2$

Therefore, $I_L = \frac{V_{in} + 2V_2 - 2V_2}{R}$ Or, $I_L = \frac{V_{in}}{R}$

Thus, the current I_L is proportionate to voltage.

1.10 CURRENT TO VOLTAGE (C TO V) CONVERTER:

Consider the simple Op-Amp circuit to convert *I* to *V*, as shown in the following Figure.



Since, current through the Op-Amp is negligible, $I_S = I_f$

$$I_s = I_f = \frac{V_B - V_0}{R_f}$$

By virtual ground concept; as node A is grounded, node B will be virtually grounded. Therefore, $V_B = 0$.

$\therefore I_s = \frac{-V_0}{R_f}$ Or, $V_0 = I_S R$

Thus, output is proportional to the input currentI_s $Reject$, and the circuit works as I to V converter.

Module 1
Chapter 3: Voltage Regulators

INTRODUCTION

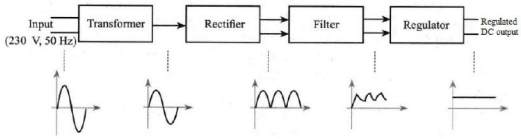
All electronic systems that we use daily, requires a stable power supply voltage source; and voltage regulators accomplish that. *Voltage regulator* is a circuit that keeps the output voltage constant under all operating conditions. *Voltage regulation* is the process of keeping a voltage steady under conditions of changing applied voltage, changing load and temperature. There are *two types* of voltage regulators: *shunt* and *series*.

1.11 Need for Regulators:

In ordinary power supplies, the voltage regulation is very poor. The DC output voltage changes appreciably with change in load current. The output voltage also changes due to fluctuations in the input AC supply. This is due the following reasons:

1. In practice, there are considerable fluctuations in line voltage caused by external factors. This changes the DC output voltage. Most of the electronic circuits will refuse to work satisfactorily on such output voltage fluctuations. Hence, regulated power supply is the solution.
2. The internal resistance of ordinary power supply is relatively large (> 30 Ω). Therefore, output voltage is affected by the amount of load current drawn from the supply. These variations in DC voltage may cause erratic operation of circuits. Without stable potentials, circuit performance degrades and if the variations are large enough, the components may get destroyed. In order to avoid this, regulated power supply is used.

Input to the voltage regulator is unregulated pulsating DC obtained from filter rectifier. Its output is constant DC voltage which is almost ripple free. The following Figure shows block diagram of regulated power supply.



The *transformer* provides voltage transformation and electrical isolation between the input power supply (AC mains) and the DC output. The *rectifier circuit* changes the AC voltage appearing across the transformer secondary to DC (unidirectional output). The rectifier circuit always has some AC content known as ripple. The *filter circuit* smoothens the ripple of the rectifier circuit. The *regulator* is a type of feedback circuit that ensures that the output DC voltage does not change from its nominal value due to change in line voltage or load current.

Factors Affecting the Load Voltage:

The variables affecting the load voltage in a power supply are given below:

1. ***Load current (IL):*** Ideally the output voltage should remain constant in-spite of changes in the load current, but practically the power supply without regulator, the load voltage decreases as load current, *IL*, increases. For practical power supply regulator, the load voltage must be constant through load to full load condition.

2. ***Line voltage:*** The input to the rectifier is AC (230 V) is the line voltage. This input decides the output voltage level. If input changes, output also changes. So this affects the performance

of power supply. So ideally voltage must remain constant irrespective of any changes in the line voltage.

3. ***Temperature:*** In the power supply, the rectifier unit is used which uses PN-junction diode. As the diode characteristics are temperature dependent, the overall performance of the power supply is temperature dependent.

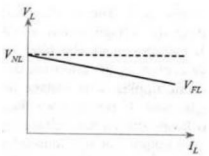
Performance Parameters of a Power Supply:

The power supply is judged by some parameters, called as *performance parameters*. These performance parameters are explained below:

1. ***Line Regulation:*** If the input to the rectifier unit i.e. 230 V changes, the output DC of rectifier will also change and since the output of rectifier is applied to the regulator, the output of regulator will also vary. Thus the source causes the change in output. This is as *source regulation* or *line regulation*. It is defined as the change in regulated DC output for a given change in input (line) voltage. Ideally the source regulation should be zero and practically it should be as low as possible.

2. ***Load Regulation:*** *Load regulation* is defined as the change in the regulated output voltage when load current is changed from zero (no load) to maximum value (full load). The load regulation ideally should be zero, but practically it should be as small as possible. The following Figure shows the load regulation characteristics.

Percentage load regulation $= \left[\frac{V_{NL}-V_{FL}}{V_{FL}}\right] * 100$



3. ***Voltage Stability factor (S_V):*** *Voltage stability factor* shows the dependency of output voltage on the input line voltage. *Voltage stability factor* is defined as the percentage change in the output voltage which occurs per volt change in input voltage, where load current and temperature are assumed to be constant. Smaller the value of this factor, better is the performance of power supply.

4. ***Temperature Stability Factor (S_T):*** As in the chain of power supply we are using semiconductor devices (diodes in rectifier block) the output voltage is temperature dependent. Thus the *temperature stability* of the power supply will be determined by temperature coefficients of various temperature sensitive semiconductor devices. So, it is better to choose the low temperature coefficient devices to keep output voltage constant and independent of temperature. *Sr* must be as small as possible, and ideally it should it should be zero for a power supply.

5. ***Ripple Rejection Factor (R_R):*** The output of rectifier and filter consists of ripples. *Ripple rejection* is defined as a factor which shows how effectively the regulator rejects the ripples and attenuates it from input to output. As ripples in the output are small compared to input, the *RR* is very small and in dB, it is in negative value.

Ripple rejection factor $= \frac{V_{RIPPLE}(OUTPUT)}{V_{RIPPLE}(INPUT)}$

When expressed in decibels, ripple rejection equals 20 log $\left[\frac{V_{RIPPLE}(OUTPUT)}{V_{R,PPLE}(INPUT)}\right] dB$

Also, $V_{RIPPLE}\ (output) = \frac{V_{RIPPLE}(INPUT)}{1+LoopGain}$

***Example*:**

Two power supplies A and B are available in the market. Power supply A has no-load and full-load voltages of 40V and 30V respectively, whereas these values are 30V and 28V for power supply B. Which one do you think is better power supply ?

Supply A: $V_{NL} = 40V, V_{FL} = 30V$

% Voltage regulation $= \left[\frac{(V_{NL}-V_{FL})}{V_{FL}}\right]^{*}100 = \left[\frac{(40-30)}{30}\right]^{*} 100 = 33\%.$

Supply B: $V_{NL} = 30V, V_{FL} = 28V$

% Voltage regulation $= \left[\frac{(V_{NL}-V_{FL})}{V_{FL}}\right] * 100 = \left[\frac{(30-28)}{28}\right]^{*} 100 = 7\%.$

Conclusion: The power supply which has lower voltage regulation is better. Hence, power supply B is between than power supply A.

Example:

A regulated power supply operates from 220 ± 20 *VAC. It produces a no-load regulated output voltage of* $24 \pm 0.5VDC$. *Also, the regulated output voltage falls from 24 VDC to 23.8 VDC as the load changes from no-load to full-load condition for the nominal value of input voltage. Determine (a) line regulation and (b) load regulation.*

Line regulation $= \frac{(24.5-23.5)}{24} = \frac{1}{24} = 0.0417 = 4.17\%$

Load regulation $= \frac{(24-23.8)}{23.8} = \frac{0.2}{23.8} = 0.0084 = 0.84\%$

Example:

A regulated power supply provides a ripple rejection of –80dB. If the ripple voltage in the unregulated input were 2V, determine the output ripple.

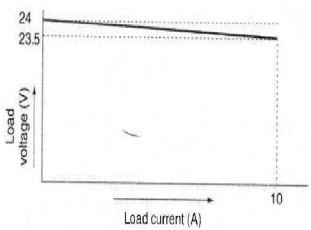
Ripple rejection in dB is given by: $20 \log \left[\frac{V_{RIPPLE}(OUTPUT)}{V_{RIPPLE}(INPUT)}\right] \text{dB} = -80\text{dB}$

$$\text{Or } \log \left[\frac{V_{RIPPLE}(OUTPUT)}{V_{RIPPLE}(INPUT)}\right] = -4$$

$$\text{Or } \left[\frac{V_{RIPPLE}(OUTPUT)}{V_{RIPPLE}(INPUT)}\right] = 10^{-4}$$

Therefore, output ripple $= 2 \times 10^{-4}\text{V} = 0.2\text{mV}$

Example: *The following Figure shows load voltage versus load current characteristics of a regulated power supply. Determine the output impedance of the power supply.*



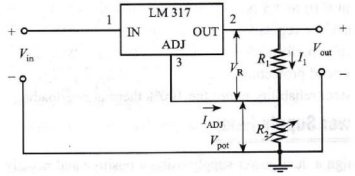
Output impedance is given by ratio of change in the output voltage for known change in the load current. From the given characteristic curve, output impedance

$= \frac{24-23.5}{10-0} = \frac{0.5}{10} = 0.05\Omega = 50m\Omega$

1.12 Adjustable Voltage Regulator:

An adjustable voltage regulator is a kind of regulator, whose regulated output voltage can be varied over a range. There are positive adjustable voltage regulators and negative adjustable regulators in practice.

LM317 is a classic example of positive adjustable voltage regulator, whose output voltage can be varied over a range of 1.2 V to 57 V. LM337, is an example of negative adjustable voltage regulator. LM337 is actually a compliment of LM317 which are similar in operation and design with the only difference being polarity of regulated output voltage.



Connection of LM317 Adjustable Voltage Regulator

The resistors R_1 and R_2 determine the output voltage V_{out}. The resistor R_2 can be adjusted to get the output voltage in the range of 1.21 V to 57 V. The output voltage is given by;

$$V_{out} = V_R (1 + R_2/R_1) + I_{ADJ}R_2$$

In this circuit, the value of the V_R is the reference voltage between the adjustment terminals and the output, taken as 1.25 Volts.

The value of I_{ADJ} will be very small and will also have a constant value. Thus the above equation can be rewritten as

$$V_{out} = 1.25(1+R_2/R_1),$$

In the equation, due to the small value of I_{ADJ}, the drop due to R_2 is neglected.

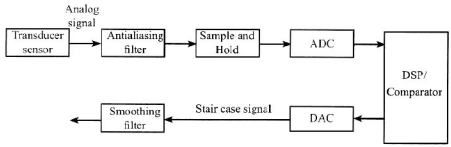
Advantages of adjustable voltage regulator over fixed voltage regulator are

1. It has adjustable output voltage form 1.2V to 57V.
2. Output current 0.10 to 1.5A
3. Better load and line regulation.
4. Improved system performance
5. Improved overload protection
6. Improved system reliability under the 100% thermal overloading.

Module 1
Chapter 4: D to A & A to D CONVERTERS

1.13 INTRODUCTION:

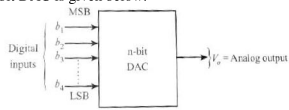
The digital system such as computers also needs to communicate with physical processes and with people through analog signals. So there is a need of digital to analog converters. Typical A/D and D/A Converter are as shown in figure below.



- Naturally available signal is analog in form, and may be obtained from *sensor or transducer*.
- This analog signal is band limited by *anti-aliasing filter.*
- The signal is then *sampled* at a frequency rate, more than twice the maximum frequency of the band limited signal. The sampled signal is held constant by *hold* circuit while conversion is taking place.
- The discrete signal from the sample and hold circuit is fed to analog to digital converter (ADC). The *ADC* gives digital output signal that can be easily processed, stored, or transmitted by digital systems or computer system.
- The digital signal is converted back to by *digital to analog converter* (DAC). The output of DAC is usually stair-case waveform, which is passed through smoothing filter to reduce the quantization noise.
- The diagram shown in the above Figure can be used in the applications such as digital signal processing, digital audio mixing, music and video synthesis, data acquisition, pulse code modulation, and microprocessor instrumentation.

1.14 BASIC DAC TECHNIQUES:

The DAC converts digital or binary data into its equivalent analog value. The symbolic representation of an n-bit DAC is given below:



The DAC output can either be a voltage or current signal. For a voltage output DAC, the conversion characteristic can be expressed by;

$$V_0 = kV_{FS}\left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots\ b_n 2^{-n}\right)$$

Where,

V_0 – Output voltage,
V_{FS} – Full scale output voltage,
k – Scaling factor (usually 1),
$b1. . ., bn$ – n-bit binary fractional word with decimal point located at the left
$b1$ – MSB with a weight = $V_{FS}/2$
bn – LSB with a weight = $V_{FS}/2^n$

Performance Parameters of DAC:

1. **Resolution:** *Resolution* is the number of various analog output values that is provided by a DAC. For n-bit DAC, $Resolution = 2^n$
   Resolution can also be defined as the ratio of change in output voltage resulting from a change of LSB at the digital input. For n-bit DAC, $Resolution = V_{OFS}/2^n - 1$.
   Where, V_{OFS} – Full scale output voltage.

   If we know the resolution, we can obtain input-output relation for DAC:

   $$V0 = Resolution \times b$$

   Where, b – Decimal values of digital input.

   For example, in a 4-bit system, using ladder, the LSB has a weight of $\frac{1}{16}$. This means that, the smallest increment in the output voltage is $\frac{1}{16}$ of the input voltage. If we assume that, this 4-bit system has input voltage levels of +16 V; (since has a weight of $\frac{1}{16}$) a change in LSB results in a change of 1 V in the output. Thus, the output voltage changes in steps of 1 V.

   Hence, this converter can be used to represent analog voltages from 0 to +15 V in 1-V increments. But, this converter cannot be used to resolve voltages into increments smaller than 1V. If we desire to produce +4.2 V, using this converter, the actual output voltage would be +4.0 V. This converter is not capable of distinguishing voltages finer than 1 V, which is the resolution of the converter.

   If we want to represent voltages to a finer resolution, we would have to use a converter with more input bits. For example, the LSB of a 10-bit converter has a weight of 1/1024. If this converter has a +10 V full-scale output, the resolution is approximately,

   $$+10 \times \frac{1}{1024} = 10mV$$

   Problem: *What is the resolution of a 9-bit D/A converter which uses a ladder network? What is the resolution expressed as a percentage? If the full-scale output voltage of this converter is +5 V, what is resolution in volts?*

   Solution:

   The LSB in a 9-bit D/A converter has a weight of $\frac{1}{512}$. Thus, this converter has a resolution of 1 part in 512.

   The resolution expressed in percentage is $\frac{1}{512} \times 100$ percent = 0.2 %.

   The voltage resolution is obtained by multiplying the weight of the LSB by the full-scale output voltage. Thus, the resolution in volts is: $\frac{1}{512} \times 5 = 10$ mV.

Problem: *How many bits are required at the input of a converter, if it is necessary to resolve voltage to 5 mV and the ladder has +10 V full-scale?*

Solution:

The LSB of an 11-bit D/A converter has a resolution of $\frac{1}{2048}$. This would provide a resolution at the output of $\frac{1}{2048} \times 10 = +5$ mV.

2. **Accuracy:** The *accuracy of the D/A converter* is primarily a function of the accuracy of the precision resistors used in the ladder and the precision of the reference voltage supply used. *Accuracy* is a measure of how close the actual output voltage is to the theoretical output value.

$$Accuracy = \frac{V_{0FS}}{\left(2^n - 1\right)2}$$

Problem: *Calculate the accuracy of a 8-bit DAC, if the full scale output voltage is 10.0 V?*
Solution:

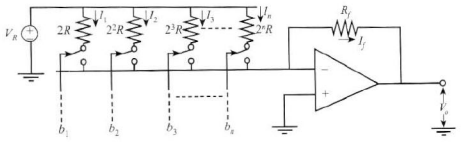
$$Accuracy = \frac{V_{0FS}}{\left(2^n - 1\right)2} = \frac{10}{\left(2^8 - 1\right)2} = 19.8mV$$

3. **Setting Time:** *Setting time* is the time required for a DAC output to settle within $\pm\frac{1}{2}LSB$ of final values for a given digital input.

4. **Stability:** The performance of a DAC is not *stable* due to the parameters such as temperature, power supply variations, and ageing.

Binary Weighted Resistor DAC:

The following Figure shows binary weighted resistor DAC circuit using *n*-electronic switches to control the binary inputs *b1, b2, . . . , bn.*



When the switch is ON; $I = \frac{V_R}{R}$, When the switch is OFF; $I = 0$.

Due to very high input impedance of Op-Amp, the total current I will flow through R_f. The total current through R_f is; $I = I_1 + I_2 + I_3 + \cdots + I_n$

$$= \frac{V_R}{2^1R}b_1 + \frac{V_R}{2^2R}b_2 + \frac{V_R}{2^3R}b_3 + \ldots + \frac{V_R}{2^nR}b_n$$

$$= \frac{V_R}{R}\left[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots + b_n 2^{-n}\right]$$

The output voltage is; $V_0 = -I_f R_f$

$$i.e.\,, V_0 = \frac{-V_R}{R}R_f\left[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots + b_n 2^{-n}\right]$$

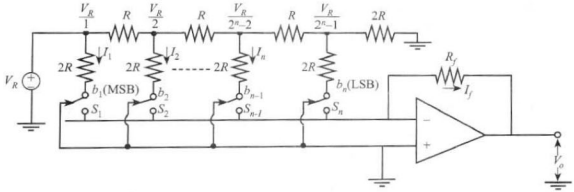
If $R_f = R$; Or, $\boldsymbol{V_0 = -V_R\left[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \; + b_n 2^{-n}\right]}$

Drawbacks:

- Large range of resistor values are required, as resistance values increases like $2^1R, 2^2R, 2^3R, \ldots, 2^nR$.
- Practically it is difficult to fabricate large values of resistors on IC.

R-2R Ladder type DAC:

In R-2R ladder, only two values, R and 2R are used. The circuit diagram is given below:



Each binary bit connects switch either to ground (non-inverting input) or to the inverting terminal of Op-Amp. Due to virtual ground, both the positions of the switches are at ground potential, and currents through the resistances are constant.

The current flowing through each of 2R resistances:

$I_1 = \frac{V_R}{2R}$, $I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R}$, $I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R}$ $I_n = \frac{V_R/(2^n-1)}{2R}$

$$\text{But, } V_0 = -I_f R_f = -R_f\left(I_1 + I_2 + \ + I_N\right)$$

$$i.e., V_0 = -R_f\left[\frac{V_R}{2R}b_1 + \frac{V_R}{4R}b_2 + \ldots + \frac{V_R}{2^n R}b_n\right]$$

$$\text{Or, } V_0 = -\frac{V_R}{R}R_f\left[b_1 2^{-1} + b_2 2^{-2} + \ + b_n 2^{-n}\right]$$

$$\text{If } R_f = R; \quad \boldsymbol{V_0 = -V_R\left[b_1 2^{-1} + b_2 2^{-2} + \ + b_n 2^{-n}\right]}$$

Advantages:

- As it requires only two types of resistors, fabrication and accurate value of R-@R can be designed.
- Node voltage remains constant, and hence, slow down effect can be avoided.

Example 1:

The Digital input for a 4bit DAC is D= 0111. Calculate its output voltage. Take V_{0FS}=15V.

Solution: $\text{Resolution} = \frac{V_{0FS}}{2^n-1} = \frac{15}{2^4-1} = 1V/LSB$

$\therefore V_0 = \text{Resolution} \times D$

$D = \text{Decimal value of } (0111) = 7$

$V_0 = \frac{1V}{LSB} \times 7 = 7V$

$\boldsymbol{V_0 = 7V}$

Example 2:

A 8bit DAC having resolution of 22mV / LSB. Calculate V_{0FS} and output of the input is $(10000000)_2$.

Given: Resolution = 22mV, Input = $(10000000)_2$.

$$\text{Resolution} = \frac{V_{0FS}}{2^n - 1}$$

$$22\text{mV} = \frac{V_{0FS}}{2^8 - 1}$$

$$V_{0FS} = 5.6V$$

D=equivalent of $(10000000)_2 = 128$

$$\boldsymbol{V_0 = 22 \times 128 = 2.8V}$$

Example 3:

Calculate output voltage produced by DAC, When output range is between 0 and 10 V for input binary number.

i) 10 (2bit DAC)
ii) 0011

Solution:

i) $V_0 = 10V\left(1 \times \frac{1}{2} + 0 \times \frac{1}{4}\right) = \mathbf{5V}$

ii) $V_0 = 10V\left(0 \times \frac{1}{2} + 0 \times \frac{1}{4} + 1 \times \frac{1}{8} + 1 \times \frac{1}{16}\right) = \mathbf{1.875\ Volts}$.

Example 4:

Calculate the values of the LSB and full scale output for 4bit DAC for 0 to 10V range.

We have, $LSB = \frac{1}{2^4} = \frac{1}{16}$

For 10V range, $LSB = \frac{10}{16} = 625mV$

And $MSB = \left(\frac{1}{2}\right) Fullscale$

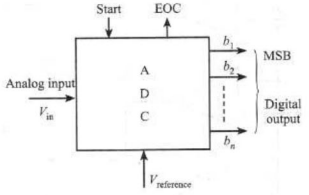
$= \frac{1}{2} \times 10 = 5V$

Full scale output = Full scale voltage – 1 LSB

=10-625mV=**9.375V**

1.15 A-D CONVERTERS:

ADC takes the analog signal as input and converts into digital output. The functional diagram of DAC is given below:

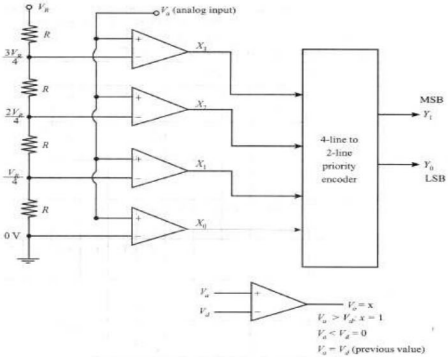


ADC is provided with two control inputs *start* (input to initiate the conversion) and *end of conversion* (output to indicate the end of conversion). *Direct type ADCs* and *Integrated type ADCs* are the two types of ADCs available.

Flash (Comparator/ Parallel) type ADC:

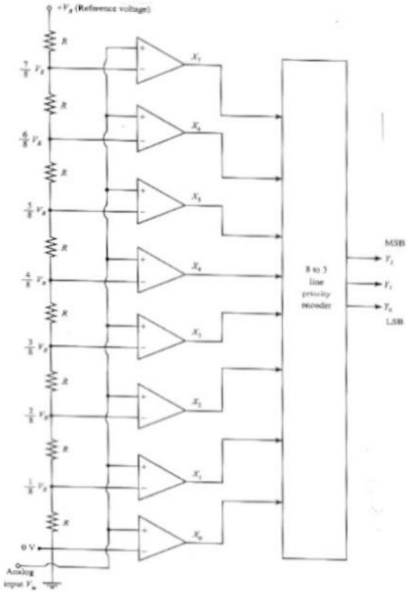
A simple, fast, but most expensive conversion technique.

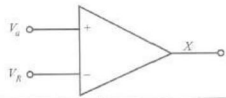
2-bit Flash ADC:



Analog input voltage (V_a)	X_3	X_2	X_1	X_0	Y_1	Y_0
0 to $\frac{V_R}{4}$	0	0	0	1	0	0
$\frac{V_R}{4}$ to $\frac{2V_R}{4}$	0	0	1	1	0	1
$\frac{2V_R}{4}$ to $\frac{3V_R}{4}$	0	1	1	1	1	0
$\frac{3V_R}{4}$ to V_R	1	1	1	1	1	1

3-bit Flash ADC:





Input voltage	Logic output (X)
$V_a > V_R$	X = 1
$V_a < V_R$	X = 0
$V_a = V_R$	Previous value

The resistive network is to set to equal reference voltages at each node. The comparator compares set reference value at inverting terminal of Op-Amp with analog output at non-inverting terminal. The truth table for ADC is given below:

Input voltage (V_a)	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $\frac{V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8}$ to $\frac{V_R}{4}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{V_R}{4}$ to $\frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8}$ to $\frac{V_R}{2}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{V_R}{2}$ to $\frac{5V_R}{8}$	0	0	0	1	1	1	1	1	0	0	0
$\frac{5V_R}{8}$ to $\frac{3V_R}{4}$	0	0	1	1	1	1	1	1	0	0	1
$\frac{3V_R}{4}$ to $\frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8}$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Advantages:
1. High speed

Disadvantages:
1. Number of comparators required is almost double for each added bit

E.g. For 2-bit ADC; No. of Comparators = 4 (2^2)
For 3-bit ADC; No. of Comparators = 8 (2^3)

Successive Approximation type ADC:

The following Figure shows successive approximation ADC.

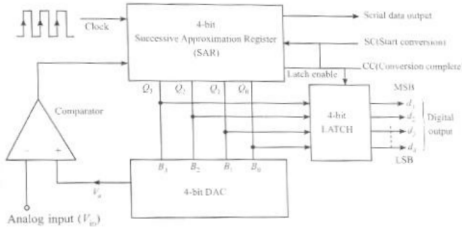
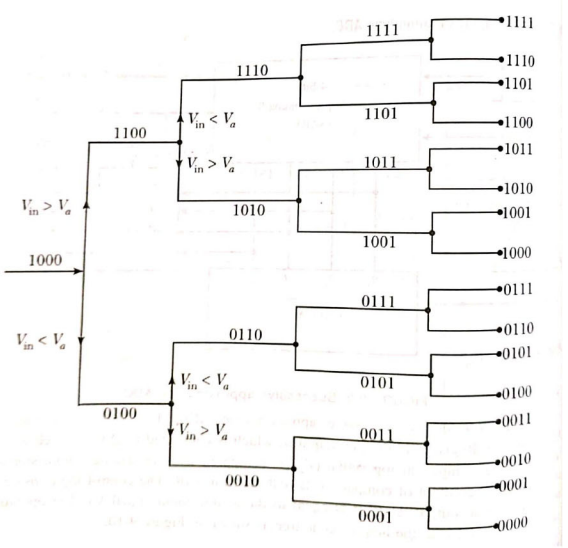


Figure shows a successive approximation register (SAR), the output of which is connected to DAC and output latch circuit. The input signal (V_{in}) is compared with the analog output signal (V_a) of the DAC. Output of the comparator is feedback into SAR. The control logic inside SAR adjusts its digital output; until it is equal to the analog input signal. The operation could be understood by the code tree given below.

At the start of conversion cycle, start conversion terminal is made high. On the first clock pulse, the output of the SAR is made 1000. The DAC produces an analog voltage (V_a) proportional to 1000. This analog voltage is compared with input analog signal (V_{in}). If V_{in}

> V_a, the comparator output will be high and SAR keeps Q3 high. On the other hand, if $V_{in} < V_a$, then the comparator output becomes low and SAR resets Q3 to low. If $V_{in} > V_a$, SAR follows the upward path in code tree and if $V_{in} < V_a$, SAR follows downward path.

The conversion time for n-bit successive approximation ADC is $(n + 2)$ clock periods.



Advantages:

1. Considerably good speed
2. Good resolution.